

Exhibit A

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

S.O.I.TEC SILCON ON INSULATOR)	
TECHNOLOGIES S.A. and SOITEC USA,)	
Inc.,)	JURY TRIAL DEMANDED
)	
Plaintiffs,)	Case No. 1:05-cv-00806-***
)	
v.)	
)	
MEMC ELECTRONIC MATERIALS, INC.,)	
)	
Defendant.		

NOTICE OF DEPOSITION

TO:

BY EMAIL AND U.S. MAIL

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TAKE NOTICE that, pursuant to Federal Rule of Civil Procedure 30, plaintiffs S.O.I.TEC SILCON ON INSULATOR TECHNOLOGIES S.A. and SOITEC USA, Inc. will take the deposition by oral examination of the individuals and entities listed on Exhibit A on the dates and at the times indicated.

The deposition of MEMC Electronic Materials, Inc. ("MEMC") referenced on Exhibit A will take place pursuant to the provisions of Federal Rule of Civil Procedure 30(b)(6), and will address the topics listed on Exhibit B. The date and time shall be the same as such individuals named on Exhibit A as MEMC may name as its corporate designee. In the event that MEMC wishes to designate an individual other than one of those named on Exhibit A as its corporate designee, the deposition of MEMC shall commence at 9:00 AM on August 18, 2007.

The deposition of Senniger Powers referenced on Exhibit A will take place pursuant to the provisions of Federal Rule of Civil Procedure 30(b)(6), and will address the topics listed on Exhibit C. One week prior to the designated date of the deposition, Senniger Powers will produce the documents specified on Exhibit D at the offices of Winston & Strawn, 35 West Wacker Drive, Chicago, Illinois 60601.

All depositions will take place at the offices of Winston & Strawn, 35 West Wacker Drive, Chicago, Illinois, 60601, and will continue from day to day, Saturdays, Sundays and holidays excluded, until completed. All depositions will be recorded by a certified stenographic court reporter authorized to administer oaths. All depositions will also be videotaped.

/s/ Michael L. Brody

Michael L. Brody

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EXHIBIT A

Full or Multi-Day Witnesses		
1.	Baccus, Bruno	9:00 AM July 26, 2007
2.	Craven, Robert	9:00 AM July 27, 2007
3.	Falster, Robert	9:00 AM July 16-17, 2007
4.	Holzer, Joseph	9:00 AM July 18, 2007
5.	Markgraf, Steve	9:00 AM July 19, 2007
6.	MEMC 30(b)(6)	In conjunction with the pertinent named deponents
7.	Mule'Stagno, Lucio	9:00 AM July 20, 2007
8.	Park, Jea-gun	9:00 AM July 24, 2007
9.	Rice, Douglas	9:00 AM July 23, 2007
10.	Senniger Powers 30(b)(6)	9:00 AM July 30-31, 2007
11.	Silicon Genesis 30(b)(6)	9:00 AM August 15, 2007
12.	Voronkov, V.V.	9:00 AM July 25, 2007
Half Day Witnesses		
1.	Banan, Mohsen	9:00 AM August 1, 2007
2.	DeLucca, John	1:30 PM August 1, 2007
3.	Goins, Tom	9:00 AM August 2, 2007
4.	Johnson, Bayard	1:30 PM August 2, 2007
5.	Kellerman, Bruce	9:00 AM August 3, 2007
6.	Kim, C.B.	1:30 PM August 3, 2007
7.	Kim, J.H.	9:00 AM August 6, 2007
8.	Kim, Y.C.	1:30 PM August 6, 2007
9.	Kimbel, Steve	9:00 AM August 7, 2007
10.	Kirk, Sue	1:30 PM August 7, 2007
11.	Lee, W.C.	9:00 AM August 8, 2007
12.	Libbert, Jeffrey	1:30 PM August 8, 2007
13.	Luter, Bill	9:00 AM August 9, 2007
14.	McCallum, Kirk	1:30 PM August 9, 2007
15.	McQuaid, Seamus	9:00 AM August 10, 2007
16.	Milvidskii, M.G.	1:30 PM August 10, 2007
17.	Mutti, Paolo	9:00 AM August 13, 2007
18.	Rowe, Blake	1:30 PM August 13, 2007
19.	Sadasivan, S.	9:00 AM August 14, 2007
20.	Schrenker, Rick	1:30 PM August 14, 2007
21.	Smolorski, Gerald	9:00 AM August 16, 2007
22.	Standley, Robert	1:30 PM August 16, 2007
23.	Vermeire, Jo	9:00 AM August 17, 2007
24.	Wilson, Greg	1:30 PM August 17, 2007

EXHIBIT B

30(b)(6) topics to MEMC

1. The development, process for manufacturing, and characterization of any low or no defect silicon wafers or device layers by MEMC Electronic Materials, Inc. ("MEMC"), including the silicon wafers referred to by MEMC as Perfect Silicon, High Performance Silicon, Semi Perfect Silicon, epitaxial silicon, annealed silicon, Advanta, Optia, or Aegis.
2. The development, process for manufacturing, and characterization of any silicon on insulator devices invented, made, sold, or marketed by MEMC.
3. The development, process for manufacturing, and characterization of silicon wafers with a region referred to by MEMC as a Magic Denuded Zone.
4. The development, process for manufacturing, and characterization of any silicon on insulator wafer comprising a device layer of material referred to by MEMC as Perfect Silicon, High Performance Silicon, Semi Perfect Silicon, epitaxial silicon, annealed silicon, Advanta, Optia, or Aegis and a handle layer that has a Magic Denuded Zone.
5. The development by MEMC of silicon wafers 300mm or more in diameter, including without limitation the development of silicon wafers 300mm or more in diameter that have "a central axis, a radius extending from the central axis to the circumferential edge, and a first axially symmetric region, in which there is a predominant intrinsic point defect, which is substantially free of agglomerated intrinsic point defects."
6. The prosecution of United States Provisional Patent Application Serial No. 60/098,902 and the prosecution of any US or foreign patent application relating to the same subject matter as the '902 application or claiming priority to the '902 application, including without limitation, United States Patent Application Serial No. 09/387,288, which issued as United States Patent No. 6,236,104. (Collectively, the "SOI Applications".)
7. The prosecution of United States Provisional Patent Application Serial No. 60/041,845 and the prosecution of any US or foreign patent application relating to the same subject matter as the '845 application or claiming priority to the '845 application, including without limitation, United States Patent Application Serial No. 09/057,851, which issued as United States Patent No. 5,919,302. (Collectively, the "Bulk Silicon Applications".)
8. The conception of any invention claimed in any patent issuing from the SOI or Bulk Silicon Applications.
9. The reduction to practice of any invention claimed in any patent issuing from the SOI or Bulk Silicon Applications.

10. Any actual or indirect infringement, either literal or under the doctrine of equivalents, by S.O.I.TEC SILCON ON INSULATOR TECHNOLOGIES S.A. and SOITEC USA, Inc. ("Soitec") of any claim of United States Patent No. 6,236,104.
11. Any allegations that any claim of United States Patent No. 6,236,104 is invalid.
12. Any allegations that any claim of United States Patent No. 6,236,104 is unenforceable.
13. Any opinion of counsel that any valid and enforceable claim of United States Patent No. 6,236,104 is infringed by declaratory judgment plaintiff Soitec.
14. MEMC's relationship with Soitec.
15. MEMC'S relationship with SiBond.
16. MEMC'S relationship with Ibis.
17. MEMC'S relationship with Silicon Genesis Corporation.
18. MEMC'S relationship with Professor Jae-gun Park or Hanyang University regarding silicon on insulator.
19. MEMC'S relationship with any person not a party to this lawsuit, including Samsung, regarding the investigation, development, manufacture, supply, sale, or marketing of silicon on insulator.
20. The testing of silicon wafers to determine the presence, type, amount and distribution of agglomerated intrinsic point defects.
21. The testing of silicon wafers to determine the presence, type, amount, and distribution of non-agglomerated intrinsic point defects.
22. MEMC'S licensing and efforts to license any patent relating to silicon wafers, silicon processing or the making of silicon on insulator, including without limitation any licensing of any patent issuing from any of the SOI or Bulk Silicon Applications.
23. Any covenant not to sue granted by MEMC to anyone relating to any patent issuing from any of the SOI or Bulk Silicon Applications.

CERTIFICATE OF SERVICE

I, Michael L. Brody, one of the attorneys of record for plaintiffs, certify that I served the foregoing Notice of Depositions on the counsel to whom it is addressed by email transmission and United States Mail on June 22, 2007 at the postal and electronic addresses indicated.

/s/ Michael L. Brody

Michael L. Brody